REMARKS

The title has been amended to conform to method nature of the pending claims.

Several changes have been made in the specification to improve or correct the grammar. The status of the additional patent application cited on page 2 has been updated to identify the patent number for that additional application.

Claims 1, 3, 4, 6 - 12, and 20 - 22 have been amended. Claims 30 - 80 have been added. Accordingly, Claims 1 - 12, 20 - 22, and 30 - 80 are now pending.

Claim 12 has been rejected under 35 USC 112 as indefinite. The Examiner alleges that the wording "semiconductor substrate and/or the first conductive layer and/or the second conductive layer" makes Claim 12 indefinite. This rejection is respectfully traversed.

Claim 12 has been amended to recite that "chemical reagent reacts with at least one of the semiconductor substrate, the first conductive layer, and the second conductive layer to form an insulator". Applicants' attorney believes that this wording satisfies the 35 USC 112 definiteness requirement. Consequently, the 35 USC 112 indefiniteness rejection should be withdrawn.

Claims 1 - 9, 20, and 22 have been rejected under 35 USC 103(a) as obvious based on Nagata et al ("Nagata"), U.S. Patent 5,804,478 B1, in view of Siniaguine et al ("Siniaguine"), U.S. Patent 6,322,903 B1. This rejection is respectfully traversed.

Nagata discloses a semiconductor memory device, specifically a dynamic RAM, in which trench-shaped groove 20 is formed in lightly doped P-type well 40 of a semiconductor body. Insulating layer 54 extends along the sidewalls and bottom of groove 20. N-type doped polysilicon (i.e., polycrystalline silicon) layer 90 is situated on insulating layer 54 and extends over the sidewalls of groove 20. N-type doped polysilicon electrode 63 lies on N-type polysilicon layer 90. Insulating layer 65 lies on N-type polysilicon electrode 63 and extends over insulating layer 54 above the bottom of groove 20. N-type doped polysilicon electrode 66 is situated on insulating layer 65 and largely fills the remainder of groove 20.

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N-type polysilicon electrodes 63 and 66 in Nagata form the plates of capacitor C1 whose capacitive dielectric is insulating layer 65. Part of electrode 66 extends above P-type well 40. Although not specified explicitly in Nagata, the portion of electrode 66 extending above well 40 is presumably connected to an electrical conductor provided above well 40 for supplying a suitable reference voltage to electrode 66. Electrode 63 is connected by way of N-type polysilicon layer 90 and N-type (monocrystalline silicon) doped region 53 to N-type source 22 of one of transfer gates Tr1 provided along the upper surface of well 40. Capacitor C1 and transfer gates Tr1 form memory cells of Nagata's dynamic RAM.

Siniaguine discloses a method for creating a vertically integrated structure in which dielectric layer 170 is provided along face side 110F of wafer 110 and covers the sidewalls and bottoms of bowl-like vias 160 that extend into face side 110F. Metal layer 150 is provided on dielectric layer 170. Back-side contact portions 150B of metal layer 150 cover the portions of dielectric layer 170 extending along the sidewalls and bottoms of vias 160. Filler material 180 fills the remaining space of each via 160. After providing contact bumps 210, conductive layer 230, and dielectric layer 410 over metal layer 150 and filler material 180, wafer 120 is bonded to wafer 110 along layers 230 and 410.

Siniaguine etches wafer 110 along its bottom side 110B for a time sufficient to reach vias 160. The portions of dielectric layer 170 extending along the bottoms of vias 160 are removed during the etch so as to expose bottom-side contacts 150B. In the resultant structure, contacts 150B protrude out of vias 160 along bottom side 110B. The remainder of insulating layer 170 also protrudes out of vias 160 along bottom side 110B but to a lesser distance than contacts 150B.

Claim 1, as amended, recites:

> 1. A circuit manufacturing method comprising:
>
> providing a structure in which an opening extends into a first side of a semiconductor substrate having a second side opposite the first side such that the opening penetrates partway through the substrate, a plurality of conductive layers overlay one another in the opening, and the conductive layers include a first conductive layer and a second conductive layer overlaying the first conductive layer such that the first and second conductive layers (i) are separated by insulating material in the

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opening, or (ii) form a P-N junction in the opening, or (iii) form a Schottky junction in the opening;

removing material along the second side of the substrate to reach the opening and expose the second conductive layer from the second side of the substrate.

The Examiner notes that Nagata does not teach "removing material from a second side of the substrate to expose the second conductive layer in the opening on the second side of the substrate". After asserting that Siniaguine discloses "a method of forming an integrated circuit, wherein a material is removed from a second side of the substrate to expose a second conductive layer in the opening on the second side of the substrate" and that "The exposed portion of the second conductive layer" in Siniaguine "serves as a contact pad", the Examiner alleges that "To connect the integrated circuit of Nagata et al. to another integrated circuit, one having ordinary skill in the art would have been motivated to modify Nagata et al. by removing material from a second side of the substrate to expose the second conductive layer in the opening on the second side of the substrate, as taught by Siniaguine et al." This allegation is illogical.

As indicated above, electrode 66 of capacitor C1 in Nagata extends above P-type well 40 and appears to be connected to an electrical conductor provided over well 40 for supplying a reference voltage to electrode 66. Providing another electrical connection to electrode 66 would serve no useful purpose and might even be damaging. For example, inconsistencies in the two voltages provided to electrode 66 might impair the performance of the memory cells of Nagata's dynamic RAM. Since electrode 66 appears to be connected to an electrical conductor provided above well 40, there would be no reason for exposing electrode 66 along the bottom of Nagata's semiconductor body in order to allow electrode 66 to be connected to another electrical conductor along the bottom of the semiconductor body. Consequently, there would be absolutely no motivation for applying the teachings of Siniaguine to the disclosure of Nagata in an effort to reach the subject matter of Claim 1.

The same is true in the (unlikely) event that electrode 66 is not connected to an electrical conductor provided over well 40 and thus that electrode 66 is floating. In that case, no useful purpose would be served by exposing electrode 66 along bottom of Nagata's semiconductor body so as to allow electrode 66 to be connected to an electrical conductor along the bottom of the semiconductor body. Doing so might even cause damage. Hence,

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there would again be no motivation for combining Nagata and Siniaguine in an attempt to reach the invention of Claim 1.

In regard to the Examiner's allegation that "one having ordinary skill in the art would have been motivated to modify Nagata et al. by removing material from a second side of the substrate to expose the second conductive layer in the opening on the second side of the substrate, as taught by Siniaguine et al" in order "To connect the integrated circuit of Nagata et al. to another integrated circuit", nothing in Nagata and/or Siniaguine would provide a person skilled in the art with such motivation. Again, there would be absolutely no need to provide electrode 66 with an electrical connection from the bottom of Nagata's semiconductor body. Claim 1 is not obvious based on Nagata and Siniaguine. Accordingly, Claim 1 is patentable over Nagata and Siniaguine.

Claims 2 - 9 all depend (directly or indirectly) from Claim 1. The same applies to Claim 12 and to new Claims 30 - 62. Hence, dependent Claims 2 - 9, 12, and 30 - 62 are patentable over Nagata and Siniaguine for the same reasons as Claim 1.

In addition, neither Nagata nor Siniaguine discloses or suggests the further limitation of any of dependent Claims 3, 9, 12, 31, 32, 34 - 38, 41, 43, 44, 47, 48, 51, 53, 55, and 58 - 62. Even if it were reasonable to combine Nagata and Siniaguine, the combination would not teach the full subject matter of any of Claims 3, 9, 12, 31, 32, 34 - 38, 41, 43, 44, 47, 48, 51, 53, 55, and 58 - 62. As a result, Claims 3, 9, 12, 31, 32, 34 - 38, 41, 43, 44, 47, 48, 51, 53, 55, and 58 - 62 are separately allowable over Nagata and Siniaguine. The same applies to Claims 45, 46, 49, 50, 56, and 57 since they variously depend (directly or indirectly) from Claims 43, 48, and 55.

Independent Claim 20, as amended, recites:

> 20. A circuit manufacturing method comprising:
>
> forming an opening in a first side of a semiconductor substrate having a second side opposite the first side such that the opening penetrates partway through the substrate;
>
> forming at least three conductive layers overlaying one another in the opening such that each consecutive pair of the conductive layers (i) are separated by insulating material in the

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opening, or (ii) form a P-N junction in the opening, or (iii) form a Schottky junction in the opening; and

removing material along the second side of the substrate to reach the opening and expose at least one of the conductive layers from the second side of the substrate.

Comments similar to what was said above about Claim 1 in regard to the attempted combination of Nagata and Siniaguine apply to Claim 12 with respect to combining Nagata and Siniaguine. For the reasons given above, nothing in Nagata and Siniaguine would provide a person skilled in the art with any motivation to expose electrode 66 along the bottom of Nagata's semiconductor body for enabling electrode 66 to be connected to an electrical conductor along the bottom of the semiconductor body.

Also, as mentioned above, electrode 63 and N-type polysilicon layer 90 are connected to transfer gate Tr1 along the upper surface of well 40. There would be no reason for connecting electrode 63 or N-type layer 90 to another electrical conductor along the bottom of Nagata's semiconductor body. Nothing in Nagata and/or Siniaguine would furnish a person skilled in the art with any motivation for exposing electrode 63 or/and N-type layer 90 along the bottom of Nagata's semiconductor body in order to enable electrode 63 or layer 90 to be connected to an electrical conductor along the bottom of the semiconductor body. Claim 20 is not obvious based on Nagata in view of Siniaguine. Hence, Claim 20 is patentable over Nagata and Siniaguine.

Furthermore, Nagata does not disclose the limitation of Claim 20 that each consecutive pair of the three conductive layers (i) be separated by insulating material, or (ii) form a P-N junction in the opening, or (iii) form a Schottky junction in the opening. Adjoining doped polysilicon layers 63 and 90 in Nagata do not form a P-N junction since layers 63 and 90 are both of N-type conductivity. Doped monocrystalline silicon region 53 in Nagata is likewise of N-type conductivity and does not form a P-N junction with adjoining layer 63. Layer 63 does not form a Schottky junction with layer 90 or region 53. Nor is layer 63 separated from layer 90 or region 53 by insulating material.

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Siniaguine does not disclose the limitation of Claim 20 that each consecutive pair of the three consecutive layers (i) be separated by insulating material in the opening, or (ii) form a P-N junction in the opening, or (iii) form a Schottky junction in the opening. Nagata and

Siniaguine would not teach the full subject matter of Claim 20 even if it were reasonable to combine the two references. This establishes a separate basis for allowing Claim 20 over Nagata and Siniaguine.

Claim 22 depends from Claim 20. New Claims 63 - 80 similarly depend (directly or indirectly) from Claim 20. Accordingly, dependent Claims 22 and 63 - 80 are patentable over Nagata and Siniaguine for the same reasons as Claim 20.

Additionally, neither Nagata nor Siniaguine discloses or suggests the further limitation of any of dependent Claims 22, 64, 65, 67, 69, 70, 72 - 76, 78, and 79. Even if it were reasonable to combine Nagata and Siniaguine, the combination would not teach the full subject matter of any of Claims 22, 64, 65, 67, 69, 70, 72 - 76, 78, and 79. Hence, Claims 22, 64, 65, 67, 69, 70, 72 - 76, 78, and 79 are separately allowable over Nagata and Siniaguine. The same applies to Claim 77 since it depends from Claim 76.

Each of Claims 10, 11, and 21 has been objected to as being dependent upon a rejected base claim but as being allowable if rewritten in independent form.

Claims 10 and 11 both depend (directly or indirectly) from Claim 1. Claim 21 depends from Claim 20. Inasmuch as Claims 1 and 20 have been shown to be patentable over the applied art, dependent Claims 10, 11, and 21 are allowable in their current form.

In summary, Claims 1 - 9, 12, 20, 22, and 30 - 80 have been shown to be patentable over the applied art. Claims 10, 11, and 21 are allowable in their current form. Consequently, Claims 1 - 12, 20 - 22, and 30 - 80 should be allowed so that the application may proceed to issue.

Please telephone applicants' attorney at 408-453-9200, ext. 1371, if there are any questions.

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Respectfully submitted,

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APPENDIX

CLAIMS 1, 3, 4, 6 – 12, AND 20 – 22,

WITH ANNOTATIONS TO INDICATE REVISIONS,

OF U.S. PATENT APPLICATION 09/941,447,

ATTORNEY DOCKET NO. M-9999-1D US

1. (Amended) A circuit manufacturing method comprising:

providing a structure in which [forming] an opening extends into [in] a first side of a semiconductor substrate having a second side opposite the first side such that the opening penetrates partway through the substrate, [with] a plurality of conductive layers overlay one another [overlaying each other] in the opening, and the conductive layers include [including] a first conductive layer and a second conductive layer overlaying the first conductive layer such that the first and second conductive layers [either] (i) are separated by [an] insulating material [layer] in the opening, or (ii) form a P-N junction in the opening, or (iii) form a Schottky junction in the opening;

removing material along the [from a] second side of the [semiconductor] substrate to reach the opening and expose the second conductive layer from [in the opening on] the second side of the substrate.

3. (Amended) The method of Claim 1 wherein the first conductive layer in the opening shields the substrate from an electromagnetic field created by an AC signal carried by the second conductive layer in the opening during circuit operation [of the circuit].

4. (Amended) The method of Claim 1 further comprising, before forming the first conductive layer, forming a primary [an] insulating layer in the opening to insulate the first conductive layer from the substrate in the opening.

6. (Amended) The method of Claim 1 wherein:

the semiconductor substrate is processed to provide an integrated circuit;[,] and

an exposed portion of the second conductive layer serves as a contact pad of the integrated circuit.

7. (Amended) The method of Claim 1 wherein:

the semiconductor substrate is processed to provide an integrated circuit;[,] and

an exposed portion of the second conductive layer serves as an input, output, or input/output terminal of the integrated circuit.

8. (Amended) The method of Claim 1 wherein:

removing material along [from] the second side of the substrate comprises mechanical removal of the material;[,] and

[wherein] the second conductive layer is exposed in the opening from [on] the second side of the substrate during the mechanical removal of the material.

9. (Amended) The method of Claim 8 wherein the mechanical removal of the material comprises chemical mechanical polishing.

10. (Amended) The method of Claim 1 wherein:

the conductive layers include a third conductive layer overlaying the second conductive layer so as to substantially fill remaining space of [and filling] the opening; [and]

[wherein] removing [removal of the] material along [from] the second side of the substrate comprises mechanical removal of the material;[,] and

[wherein] the third conductive layer is exposed in the opening from [on] the second side of the substrate during the mechanical removal of the material.

11. (Amended) The method of Claim 10 wherein:

the mechanical removal of the material is followed by etching the substrate along its [an etch of material on the] second side;[,] and

[wherein] at least one of the second and third conductive layers protrudes from the opening along [on] the second side of the substrate after the etch.

12. (Amended) The method of Claim 1 wherein:

after [the] removing [of the] material along the second side of the substrate, the first and second conductive layers are exposed in the opening from [on] the second side of the substrate; and

[wherein] the method further comprises, after [said] removing [of the] material along the second side of the substrate, processing the second side of the substrate with [a] chemical reagent [or reagents] that reacts [react] with at least one of the semiconductor substrate [and/or], the first conductive layer [and/or], and the second conductive layer to form an insulator.

20. (Amended) A circuit manufacturing method comprising:

forming an opening in a first side of a semiconductor substrate having a second side opposite the first side such that the opening penetrates partway through the substrate;

forming at least three conductive layers overlaying one another [each other] in the opening[,] such that each [two] consecutive pair of the conductive layers [either] (i) are separated by [an] insulating material [layer] in the opening, or (ii) form a P-N junction in the opening, or (iii) form a Schottky junction in the opening; and

removing material along the [from a] second side of the [semiconductor] substrate to reach the opening and expose at least one of the [said] conductive layers from [in the opening on] the second side of the substrate.

21. (Amended) The method of Claim 20 wherein all of the [said] conductive layers are metal layers [which are] separated from one another [each other] by insulating material [layers] in the opening.

22. (Amended) The method of Claim 20 wherein at least two of the [said] conductive layers are connected through a permanent or programmable connection outside [of] the opening.